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| 10/723,347 | 11/25/2003 | Zohar Bogin | P17517 | 8242 |

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| EXAMINER | |
|---|---|
| MARTINEZ, DAVID E | |
| **ART UNIT** | **PAPER NUMBER** |
| 2181 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/723,347 | BOGIN ET AL. | |
| | Examiner | Art Unit | |
| | David E. Martinez | 2182 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Examiner vacated the previous restriction requirement.

### *Claim Rejections - 35 USC § 101*

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 19 and 25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims seem to be missing essential elements or steps which lead to a tangible result. As per claim 19, it seems to be missing the essential action of actually transferring data which leads to the updating of a position value. As per claim 25, it seems to be lacking the essential step of actually using the audio controller to stream the data. Merely reading data to make a determination does not appear to be a tangible result absent the missing step of using the controller to stream data. The 112 problem below leads to this 101 problem and thus correcting the 112 problem will correct the 101 problem.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 2, 6, 7, 13, 19 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regards to claim 1, lines 1-2, the term "In a controller of a computing device that comprises a system memory and a codec" renders the claim indefinite and unclear. What

comprises the system memory and a codec? Is the applicant referring to controller or the computing device?

With regards to claim 2, the term "wherein reading comprises..." renders the claims indefinite since it is not understood if something in particular is being read or if the claim is referring to the reading data from a buffer step in it's parent claim 1.

With regards to claim 6, it is not understood what is being determined. If the value is always being updated when a transfer takes place, there is no determination taking place.

With regards to claim 7, it suffers from the same deficiencies as claim 1 above and thus is rejected under the same rationale.

With regards to claim 13, line 3, the term" and a buffer position," is unclear. It is not understood if the "buffer position" is referring to a register or memory module that stores a buffer position value, or if it is referring to the relative position of the buffer with respect to the other physical components. Furthermore, on line 7, "the term updates the buffer position", is also unclear since it is not known if the applicant is referring to updating a value inside a buffer register or memory module, or if there is a change in physical position of the buffer inside the system.

With regards to claim 19, in line 5 the term "a position in *the* (typo?) buffer controller to update a position value" is unclear. Is applicant claiming a position? or is it referring to perhaps a register or some kind of memory holding a position value? Furthermore in claim 19 lines 6-7, the term "to indicate a position of the direct memory access controller in the buffer" is not understood. Is the direct memory access controller itself moving within the buffer?

With further regards to claim 19, the position buffer controller which updates a position value in some kind of register seems to necessitate the first dma controller to actually transfer

data, yet the dma controller fails to positively recite this action. It seems to be lacking the essential action of actually transferring data which leads to the updating of a position value.

With regards to claim 25, on lines 5 and 8, it suffers from the same deficiencies as those of claim 13 above and thus is rejected under the same rationale. Furthermore in claim 25, the first two steps require configuration to do something, but not actually doing it, yet the 3rd step necessitates it actually being done in order to read the requisite information. It seems to be lacking the essential step of actually using the audio controller to stream the data.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-7, 9-13, 16, 19, 20, 25, 27 and 28, are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,792,481 to Hoang et al. (hereinafter Hoang) in view of US Patent No. 6,418,489 to Mason et al. (hereinafter Mason).

1. With regards to claim 1, Hoang teaches in a controller [fig 1 element 20, details shown in fig 2] of a computing device [fig 1 system 10, column 2 lines 19-38] that comprises a system memory [fig 1 element 16] and a codec [fig 1 element 32], a method comprising

reading data from a buffer [fig 1 element 16] of the system memory [fig 1 element 16] via a first interface of the controller [fig 2 element 22, column 3 lines 28-39],

transferring the data to the codec via a second interface of the controller [fig 2 element 26, column 3 lines 28-39],

tracking a position in the buffer from which the controller has read the data [fig 2 element 78, column 3 lines 29-32, column 5 lines 45-49],

Hoang teaches storing a value in an register to indicate the position in the buffer [fig 2 elements 58 and 78, column 3 lines 21-24, column 4 lines 29-32,]. Hoang teaches all of the above limitations except for writing a value to the system memory via the first interface to indicate the position in the buffer. However, Mason teaches a controller that writes values to the system memory via an interface instead of storing them in internal registers to reduce the amount of internal hardware in the controller and improve efficiency and overall performance [column 2 line 48 to column 3 line 3, column 14 lines 19-31].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Hoang and Mason to write a value to the system memory via the first interface to indicate the position in the buffer to reduce the amount of internal hardware in the controller and improve efficiency and overall performance.

2. With regards to claim 3, Hoang teaches the method of claim 1 further comprising tracking progress of transferring the data to the codec via the second interface [column 3 lines 29-50].

3. With regards to claim 4, Hoang teaches the method of claim 1 wherein reading the data from the buffer comprises reading the data per a buffer descriptor list that defines the buffer [fig 2 elements 50, 52, 70, 72].

4. With regards to claim 5, Hoang teaches the method of claim 4 wherein reading the data from the buffer further comprises returning to a start of the buffer in response to reaching an end of the buffer [column 4 lines 24-35].

5. With regards to claim 6, Hoang teaches the method of claim 1 further comprises determining to update the value in the system memory based upon the data transferred via the second interface prior to writing the value to system memory [column 4 lines 29-32].

6. With regards to claim 7, Hoang teaches in a controller [fig 1 element 20, details shown in fig 2] of a computing device [fig 1 system 10, column 2 lines 19-38] that comprises a system memory [fig 1 element 16] and a codec [fig 1 element 32], a method comprising

receiving data from the codec [fig 1 element 32] via a first interface of the controller [figs 1, 2 element 28, column 2 lines 39-49],

writing the data to a buffer of the system memory via a second interface of the controller [figs 1 element 16, column 2 lines 39-49],

tracking a position in the buffer to which the controller has written the data [column 3 lines 29-32],

Hoang teaches storing a value in an register to indicate the position in the buffer [fig 2 elements 58 and 78, column 3 lines 21-24, column 4 lines 29-32,]. Hoang teaches all of the above limitations except for writing a value to the system memory via the second interface to indicate the position in the buffer. However, Mason teaches a controller that writes values to the system memory via an interface instead of storing them in internal registers to reduce the amount of internal hardware in the controller and improve efficiency and overall performance [column 2 line 48 to column 3 line 3, column 14 lines 19-31].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Hoang and Mason to write a value to the system memory via the second interface to indicate the position in the buffer to reduce the amount of internal hardware in the controller and improve efficiency and overall performance.

7. With regards to claim 9, it is of the same scope as claim 3 above and thus is rejected under the same rationale.

8. With regards to claim 10, it is of the same scope as claim 4 above and thus is rejected under the same rationale.

9. With regards to claim 11, it is of the same scope as claim 5 above and thus is rejected under the same rationale.

10. With regards to claim 12, it is of the same scope as claim 6 above and thus is rejected under the same rationale.

11. With regards to claim 13, Hoang teaches a system [fig 1] comprising

a processor [fig 1 element 12],

a system memory [fig 1 element 16] comprising a buffer [fig 1 element 16] and a buffer position [the combination of Hoang and Mason for the same reasons as those set forth under the claim 1 and 7 rejection above],

an audio controller [fig 1 element 20] coupled to the system memory [fig 1 element 16] via a first bus [fig 1 element 11], and

a codec [fig 1 element 32] coupled the audio controller [fig 1 element 20] via a second bus [fig 1 element 20 has the buffers and codec interfaces connected over a bus to element 32], wherein

the audio controller [fig 1 element 20] transfers data between the buffer [fig 1 element 16] and the codec [fig 1 element 32] via the first bus [fig 1 element 11] and the second bus [fig 1 element 20 has the buffers and codec interfaces connected over a bus to element 32] and updates the buffer position via the first bus to indicate a position in the buffer associated with the audio controller transferring between the buffer and the audio controller [column 4 lines 24-35].

12. With regards to claim 16, it is of the same scope as claim 4 above and thus is rejected under the same rationale. Furthermore, it would have been obvious to store the descriptor list in system memory for the same reasons set forth under the claim 1 rejection above taught by the combination of Hoang and Mason.

13. With regards to claim 19, it is of the same scope as the combination of claims 1 and 7 above and thus is rejected under the same rationale.

14. With regards to claim 20, it is of the same scope as claims 1 and 4 above, and thus is rejected under the same rationale. Furthermore, Hoang teaches the buffer descriptor list is included in the dma controller [fig 1 and 2 element 20] rather than inside the system memory. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the buffer descriptor list in the system memory for the same reasons as those set forth in the claim 1 rejection above.

15. With regards to claim 25, it is of the same scope as claim 13 above and thus is rejected under the same rationale.

16. With regards to claim 27, Hoang teaches the machine-readable medium of claim 25 wherein the plurality of instructions in response to being executed further result in the computing device

allocating the buffer in the system memory [allocating takes place when the controller (fig 1 element 20) is instructed to storing data in the system memory] and storing a buffer descriptor list in the system memory [same scope as a combination of claim 16 and 1 above thus rejected under the same rationale], and

configuring the audio controller to transfer the data per the buffer descriptor list [same scope as claim 16 and 1 above].

17. With regards to claim 28, Hoang teaches the machine-readable medium of claim 25 wherein the plurality of instructions in response to being executed further result in the computing device

allocating a position in buffer structure in the system memory [this is done when storing data in the memory buffer, the particular position must be allocated in order to be filled, ], and

configuring to update the position in buffer structure with the buffer position [same scope as in claim 1 above].

Claims 2, 8, 14, 17, 18, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,792,481 to Hoang et al. (hereinafter Hoang) in view of US Patent No. 6,418,489 to Mason et al. (hereinafter Mason) further in view of Applicant's Admitted Prior Art (hereinafter AAPA).

18. With regards to claim 2, Hoang teaches receiving the data via the first interface [fig 2 element 22, column 3 lines 28-39], but the combination of Hoang and Mason are silent as to wherein reading comprises isochronously receiving the data via the first interface. However, AAPA teaches using isochronous data transfers for the benefit of helping multimedia applications such as audio and video applications achieve high quality results [page 1, paragraph 1].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hoang, Mason and AAPA to isochronously receive the data via the first interface for the benefit of helping multimedia applications such as audio and video applications achieve high quality results.

19. With regards to claim 8, it is of the same scope as claim 2 above and thus is rejected under the same rationale.

20. With regards to claim 14, it is of the same scope as claim 2 above and thus is rejected under the same rationale.

21. With regards to claim 17, it is of the same scope as the combination of claims 1 and 2 above and thus is rejected under the same rationale.

22. With regards to claim 18, it is of the same scope as the combination of claims 7 and 2 above and thus is rejected under the same rationale.

23. With regards to claim 23, it is of the same scope as claim 2 above, when transfers are directed to writing data isochronously, and thus is rejected under the same rationale.

24. With regards to claim 24, it is of the same scope as claim 2 above, when transfers are directed to reading data isochronously, and thus is rejected under the same rationale.

Claims 15, 21, 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,792,481 to Hoang et al. (hereinafter Hoang) in view of US Patent No. 6,418,489 to Mason et al. (hereinafter Mason) further in view of US Patent No. 6,693,753 to Su et al. (hereinafter Su)

25. With regards to claim 15, Hoang teaches the system of claim 13 wherein the audio controller [fig 1 element 20] transfers the data across a link of the first bus [fig 1 element 11] but is silent as to updating a link position counter of the audio controller based upon the data transferred across the link. However, Su teaches using a link position counter in an interface between two communicating devices for the benefit of tracking the progress of the data transfer [column 7 lines 4-22].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hoang, Mason and Su to update a link position counter of the audio controller based on the data transferred across the link for the benefit of tracking the progress of the data transfer.

26. With regards to claim 21, it is of the same scope as claim 15 above and thus is rejected under the same rationale.

27. With regards to claim 22, it is of the same scope as claim 15 above and thus is rejected under the same rationale.

28. With regards to claim 26, it is of the same scope as claim 15 above and thus is rejected under the same rationale.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 5,526,353 to Henley et al. teaches data transmission between a codec and a FIFO buffer and keeping track of how full/empty the buffer is while transmitting data.

US Patent No. 5,822,553 to Gifford et al. teaches data transmission between a codec and a FIFO buffer and keeping track of how full/empty the buffer is while transmitting data.

US Patent No. 6,690,676 to Gulick et al. teaches data a DSP controller controlling the communication transmission between a codec and a buffer also see figures 8b and 8c, c

US Patent No. 5,889,480 to Kim teaches a DMA controller for transferring data between a codec and system memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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